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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/586,325	BORTFELD ET AL.	
	Examiner	Art Unit	
	Dwin M Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *36-38* is/are allowed.

6)☒ Claim(s) *1-8,10-15,17-21,23-31,33 and 34* is/are rejected.

7)☒ Claim(s) *9, 16, 22, 32 & 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-35 have been presented for reconsideration based on Applicant's amended claim language and arguments. Claims 36, 37 and 38 have been presented for Examination.

Response to Arguments

2. Applicant's arguments filed on 11-15-2004 have been fully considered. Examiners response is as follows.

2.1 Regarding the Applicants response to the 35 U.S.C. 103 rejections of Claims 1, 5-6, 10, 17, 23-24, 28-29 and 33-34 under 35 U.S.C. 103:

Applicants have argued, on page(s) 18 & 19 of the 11-15-2004 responses:

> Hollander does not teach, disclose, or suggest creating models of components and a set of function calls in a high level general purpose programming language and executing a virtual prototype, where models communicate through a transaction based interconnect and cycle accurate information is generated, and where the transaction based interconnect includes a set of function calls.

...and on page 19,

> ...Dearth does not teach, disclose, or suggest creating models of components and a set of function calls in a high level general purpose programming language and executing a virtual prototype, where models communicate through a transaction based interconnect and cycle accurate information is generated, and where the transaction based interconnect includes the set of function calls.

...and on page 20,

> However, a hardware description language is not the same as a high level general purpose programming language, as specified in amended claim 1.

The Examiner has found Applicant's arguments to be persuasive in that neither the *Dearth* or *Hollander* reference teach or make obvious the limitation of *creating models of said components in a high level general purpose programming language.* The *Dearth* and *Hollander* reference disclose creating the models using a hardware description language. The Applicant has clearly argued that the claimed limitation of using a high level programming language excludes the use of a hardware description language. The Examiner has found this argument to be persuasive and agrees with the Applicant that neither the *Dearth* nor the *Hollander* reference disclose the use of a high level general purpose programming language to model a component in the simulation of a system. The Examiner withdraws the earlier 35 U.S.C. 103(a) rejections of claims 1, 5-6, 10, 17, 23-24, 28-29 and 33-34 under 35 U.S.C. § 103(a).

Based on Applicant's amended claim language and arguments an updated search has revealed new art.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Independent **Claims 1, 10, 17, 23 and 33** and **dependent Claims 2-8, 11-15, 18-21, 24-31 and 34** are rejected under 35 U.S.C. 102(b) as being anticipated by **Stapleton U.S. Patent 5,870,585.**

3.1 As regards independent **Claims 1, 10, 17, 23 and 33** the *Stapleton* reference discloses;

a computer method for simulating a system design **(Col. 2 Lines 12-24,** *note that the "objects" or "modules" discussed in the Summary of the Invention are a "system"***),**

containing at least two components **(Figure 4** Items 401 and 402, **Figure 3** Items 302 and 301**),**

and creating models of said components in a high level general purpose programming language **(Figure 1** items 106 & 107**, and Col. 5 Lines 1-29 and Col. 2 Lines 37-44),**

creating a set of function calls **(Figure 2** item 204, **Col. 2 Lines 45-54, Appendix A and Col. 6 Lines 38-47),**

a virtual prototype **(Figure 3, Col. 7 Lines 27-67, Col. 8 Lines 1-13,** *note that the circuit disclosed in figure 3 is not an "actual" circuit built in hardware but a "virtual" circuit that only exists in the simulation until the actual hardware is created at the end of the design process***),**

a transaction based interconnect **(Col. 8 Lines 47-49** *the base class vector is functionally equivalent to a transaction based interconnect***),** and cycle accurate information **(Col. 3 Lines 35-38),** is generated where in said transaction based interconnect includes a set of function calls **(Figure 2** item 204 labeled "LD_NEW_STATE() and GEN_NEWSTATE(), **Figure 5,** and **Col. 5, lines 30-67 and Col. 6 Lines 1-37).**

Further, the *Stapleton* reference discloses the *"initialization of the model(s)"* **(Col. 2 Lines 25-27, Col. 10 Lines 28-50),** which is functionally equivalent to "identifying" a component.

3.2 As regards dependent **Claims 2, 11, 18 and 25** the *Stapleton* reference inherently teaches the creation of a *"blank component model"*, it is noted by the Examiner that the

Stapleton reference discloses the use of Object Oriented Programming methods which *inherently* provides for the use of a *"default constructor" see also* **(Col. 8 lines 62-67, Col. 9 lines 1-33),** when an object model is instantiated using the *"new"* command. As regards the limitation of adding *"subcomponents"* see **(Figure 4 items 401 and 402),** as regards configuring the subcomponents with parameters see **(Col. 8 Lines 20-45).**

3.3 As regards dependent **Claims 24 and 34** the *Stapleton* reference teaches a high level programming language **(Col. 2 Lines 37-44).**

3.4 As regards dependent **Claims 3, 8, 12, 26 and 31** the *Stapleton* reference teaches sub-components **(Figure 4 items 401 & 402),** and linking function calls with the sub-components **(Col. 8 Lines 20-45).**

3.5 As regards dependent **Claims 4, 7, 13, 19, 27 and 30** the *Stapleton* reference *inherently* teaches a *component repository* because, the software classes when they are instantiated, will store the components in system memory and provide a pointer to the objects in memory, thus providing a repository where a modeled component can be stored and retrieved.

3.6 As regards dependent **Claims 5, 6, 14, 15, 20, 21, 28 and 29** the *Stapleton* reference teaches control interfaces **(Figure 2 item** "SETCHPIO"**),** peer interfaces **(Figure 2** item "DO_ONE_CHP_CYCLE"**),** clock functions **(Col. 7 lines 26-40),** access functions **(Figure 2 item 205** *"getting results is providing access"*), and signal functions **(Figure 4 item 403** "`Wire: int w1;`" and **Col. 8 Lines 20-31).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Independent **Claims 1, 10, 17, 23, 33 and** dependent **Claims 2-8, 11-15, 18-21, 24-31 and 34** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Saitoh et al. U.S. Patent 6,154,719** in view of **Parson U.S. patent 6,053,947.**

4.1 As regards independent **Claims 1, 10, 17, 23 and 33** the *Saitoh et al.* reference discloses; a computer method for simulating a system design **(Figure 7),** creating models **(Figure 4 item 13),** containing at least two components **(Col. 10 Lines 15-43),** a virtual prototype **(Figure 7** discloses the functional equivalent of the *"virtual prototype"* because the design is in a computer memory**).**

However, the *Saitoh et al.* reference does not expressly disclose, using a high level general purpose programming language, creating and linking a set of function calls and transaction based interconnects including a set of function calls.

The *Parson* reference discloses using a high level general purpose programming language to model circuit components in a simulation **(Figure 4 items 401b & 402b),** creating and linking a set of function calls **(Figure 3, Col. 6 lines 46-67, Col. 7 lines 1-17),** and transaction based interconnects including a set of function calls **(Figures 5, 6 & 8 and Col. 9 lines 22-29).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have used the high level programming language methods disclosed in the *Parson* reference to model the system with a plurality of components disclosed in the *Saitoh et al.* reference because by using a high level programming language to model the components instead of the hardware description language used in the *Saitog et al.* reference, faster simulation speed can be realized **(Parson Col. 29 lines 58-67, Col. 29 lines 1-10).**

4.2 As regards dependent **Claims 2, 11, 18 and 25** the *Saitoh et al.* reference discloses components and subcomponents **(Figure 7).**

4.3 As regards **Claims 24 and 34** the *Saitoh et al.* reference does not expressly disclose using a high level general purpose programming language.

The *Parson* reference discloses using a high level general purpose programming language **(Figure 4 item 401B).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have used the high level programming language methods disclosed in the Parson reference to model the system with a plurality of components disclosed in the *Saitoh et al.* reference because by using a high level programming language to model the components instead of the hardware description language used in the *Saitog et al.* reference, faster simulation speed can be realized **(Parson Col. 29 lines 58-67, Col. 29 lines 1-10).**

4.4 As regards dependent **Claims 3, 8, 12, 26 and 31** the *Saitoh et al.* reference discloses components and subcomponents **(Figure 7),** however, the *Saitoh et al.* reference does not expressly disclose using function calls to link the components.

The *Parson* reference discloses the use of function calls *(object methods)* to link different components in a simulation **(Figure 7 item 701, Col. 15 Lines 64-67, Col. 16 lines 1-18).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have used the high level programming language methods disclosed in the Parson reference to model the system with a plurality of components disclosed in the *Saitoh et al.* reference because by using a high level programming language to model the components instead of the hardware description language used in the *Saitog et al.* reference, faster simulation speed can be realized **(Parson Col. 29 lines 58-67, Col. 29 lines 1-10).**

4.5 As regards dependent **Claims 4, 7, 13, 19, 27 and 30** the *Saitoh et al.* reference discloses a component repository **(Figure 4 item 14).**

4.6 As regards dependent **Claims 5, 6, 14, 15, 20, 21, 28 and 29** the *Saitoh et al.* reference does not expressly disclose control interfaces, peer interfaces, clock functions, access functions and signal functions.

However, the *Parson* reference discloses control interfaces **(Col. 17 lines 58-65),** peer interfaces **(Figures 5 & 6Col. 8 lines 40-45),** clock functions (**Figure 3 item 304**), access functions **(Col. 17 lines 66-67, Col. 18 lines 1-8),** and signal functions **(Figures 5, 6, 9 & 10).**

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have used the high level programming language methods disclosed in the Parson reference to model the system with a plurality of components disclosed in the *Saitoh et al.* reference because by using a high level programming language to model the components instead of the hardware description language used in the *Saitog et al.* reference, faster simulation speed can be realized **(Parson Col. 29 lines 58-67, Col. 29 lines 1-10).**

Allowable Subject Matter

5. **Claims 9, 16, 22, 32 and 35** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5.1 **Claims 36, 37 and 38** are allowed.

Conclusion

6. **Claims 1, 10, 17, 23 & 33** and dependent **Claims 2-8, 11-15, 18-21, 24-31 and 34** are rejected. **Claims 9, 16, 22, 32 and 35** are objected to. This action is **NON-Final.**

6.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

Dwin Craig's E-Mail address is: craig.dwin@uspto.gov

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (571)272-3716.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER